DATA SHEET

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SR8824

24 CHANNEL PARALLEL CORRELATOR CIRCUIT FOR GPS AND GLONASS RECEIVERS

FEATURES

- ❑ 24 Fully Independent Correlation Channels
- ❑ Switchable to Receive GPS or GLONASS Codes
- ❑ Input Multiplexer for Multiple GPS Front-Ends – Allows Antenna Diversity
- ❑ Input Multiplexer for GLONASS Multiple (Separate Channels) Front-Ends
- ❑ On-Chip Dual UART and Real Time Clock
- ❑ Fully Compatible with GP2010, GP2015 GPS Receiver Front-End
- ❑ Memory and peripheral control logic for AD2106x micro processors
- ❑ 144-pin Plastic Quad Flatpack
- ❑ Power Dissipation Less Than 100mW

APPLICATIONS

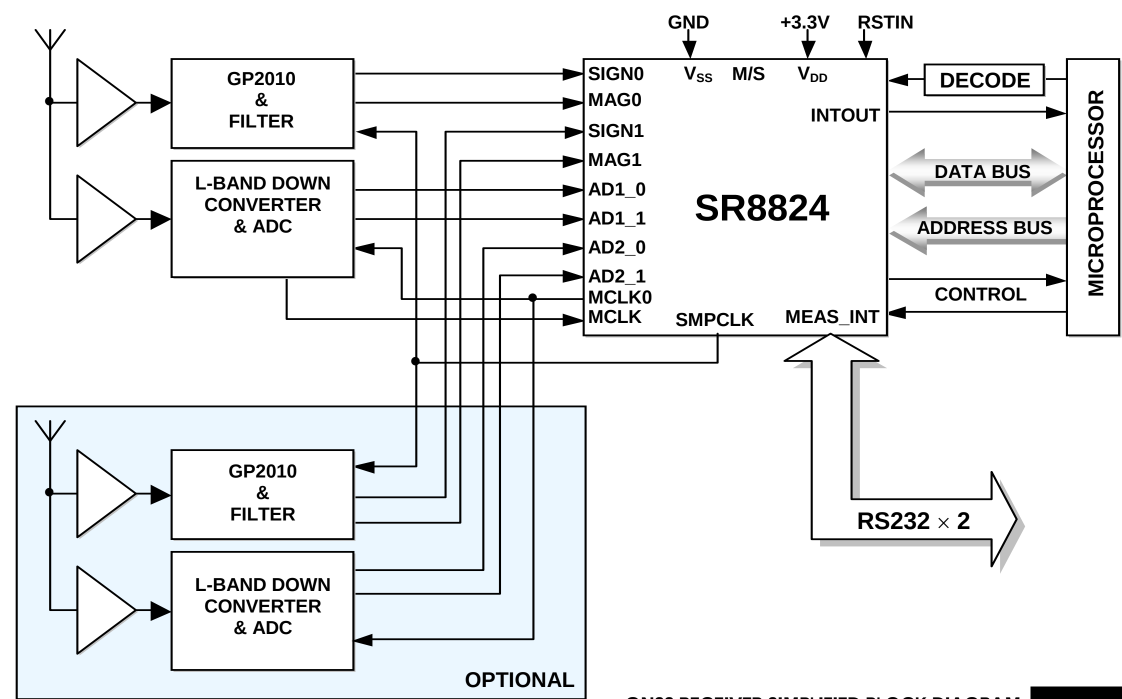
- ❑ GNSS Navigation Systems
- ❑ High Integrity Combined Receivers
- ❑ GNSS Geodetic Receivers
- ❑ GNSS Time Reference

TYPICAL GNSS RECEIVER (see Fig. 1)

All GPS satellites use the same L1 frequency of 1575·42MHz, but different Gold codes, so a single front-end may be used.

Each GLONASS satellite will use a different ‘L1’ carrier frequency, in the range 1598·0625 to 1615·500MHz, with 0·5625MHz spacing, but all with the same 511-bit spreading code, so wide-band receiver used with a single front-end.

To achieve better sky coverage it may be desirable to use more than one antenna, in which case separate front-ends will be needed.



GNSS RECEIVER SIMPLIFIED BLOCK DIAGRAM **FIGURE 1**

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VDD	I/O supply voltage	2.97	3.3	3.63	V
V_{IH}	Input High Voltage	2.0	—	5.5	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
VT	Threshold point	1.45	1.58	1.74	V
VT+	Schmitt trig Low to High threshold point	1.44	1.50	1.56	V
VT-	Schmitt trig. High to Low threshold point	0.89	0.94	0.99	V
I_L	Input Leakage Current	—	—	±10	µA
IOZ	Tri-State output leakage current	—	—	±10	µA
RPU	Pull-up Resistor	39	65	116	kΩ
RPD	Pull-down Resistor	40	56	108	kΩ
V_{OL}	Output low voltage IOL=2,4…24mA	—	—	0.4	V
V_{OH}	Output high voltage IOH=2,4…24mA	2.4	—	—	V
I_{OL}	Low level output current VOL=0.4V 2mA	2.4	4.0	5.0	mA
	4mA	4.7	8.0	10	mA
	8mA	9.4	15.9	19.8	mA
	12mA	14.2	23.9	29.8	mA
	16mA	18.9	31.8	39.8	mA
	24mA	28.3	47.8	59.7	mA
I_{OH}	High level output current VOH=2.4V 2mA	2.8	5.9	9.5	mA
	4mA	5.6	11.9	19	mA
	8mA	11.2	23.8	38.3	mA
	12mA	16.8	35.7	57	mA
	16mA	22	47.7	76	mA
	24mA	33.7	71.5	115	mA

PIN DESCRIPTIONS

NOTE 1. 10µF and 0.01µF ceramic bypass capacitor is required to externally connect between VDDint and GND.

NOTE 2. 4.7µF ceramic bypass capacitor is re-

NOTE 3. The functions of RW and WEN pins depend on whether the GP1020 is in Motorola™ (MOT/INTEL = '1') or Intel™ mode (MOT/INTEL = '0'). In Motorola mode, WEN is an enable (active high) and RW is Read/Write select ('1' = Read). In Intel mode RW is Read, active low, and WEN is Write also active low.

V_{SS}	10, 19, 21, 23, 36, 46, 66, 67, 72, 86, 109, 127, 133, 143
V_{DD} (3.3V)	9, 25, 40, 56, 73, 91, 118, 138, 144
$V_{DD\ INT}$ (3.3V)	128, 129
VREF_1.8 (Output 1.8V)	130
GND	131, 132

NOTE 4. WRPROG is used to modify the timing of bus operations; when it is held HIGH the internal write signal is ORed with ALE to allow time for the internal address lines to stabilize; when it is held LOW there is no delay added to write.

NOTE 5. All V_{SS} and all V_{DD} pins must be used in order to ensure reliable operation.

TABLE 1

PIN No.	PIN NAME	BUFFER TYPE	DIREC-TION	DESCRIPTION
1	**IED0**	PISUN	I	External Data Input 0
2	**IED1**	PISUN	I	External Data Input 1
3	**IED2**	PISUN	I	External Data Input 2
4	**IED3**	PISUN	I	External Data Input 3
5	**IED4**	PISUN	I	External Data Input 4
6	**IED5**	PISUN	I	External Data Input 5
7	**IED6**	PISUN	I	External Data Input 6
8	**IED7**	PISUN	I	External Data Input 7
9	VDD			
10	VSS		I	
11	**ADI2_1**	PIUN	I	GL SV Input I2_1
12	**ADQ2_1**	PIUN	I	GL SV Input Q2_1
13	**ADI2_0**	PIUN	I	GL SV Input I2_0
14	**ADQ2_0**	PIUN	I	GL SV Input Q2_0
15	**ADI1_1**	PIUN	I	GL SV Input I1_1
16	**ADQ1_1**	PIUN	I	GL SV Input Q1_1
17	**ADI1_0**	PIUN	I	GL SV Input I1_0
18	**ADQ1_0**	PIUN	I	GL SV Input Q1_0
19	VSS			
20	**CLK40D**	PINN	I	40 MHz Clock (UART)
21	VSS			
22	**MCLK**	PINN	I	40 MHz Master Clock
23	VSS			
24	**MCLKO**	PO8N	O	40 MHz Output
25	VDD			
26	**PMCLK**	PIUN	I	Polarity MCLKO
27	**SMPCLK**	PO8N	O	Sampling clock to down-converter
28	**RTCINT**	PISUN	I	Real time clock interrupt input
29	**SIGN1**	PIUN	I	Satellite Input 1, Sign
30	**MAG1**	PIUN	I	Satellite Input 1, Magnitude
31	**SIGN0**	PIUN	I	Satellite Input 0, Sign
32	**MAG0**	PIUN	I	Satellite Input 0, Magnitude
33	**MS1**	PINN	I	ROM addr. pre decode strobe
34	**MS3**	PINN	I	Correlator addr. pre decode strobe
35	**MS2**	PINN	I	Interfaces addr. pre decode strobe
36	VSS			
37	**BITECNTL**	POL8N	O	BITE control to down-converter GPS
38	**PLLLOCKN**	PIUN	I	PLL lock status from down-converter
39	**GLBIT**	POL8N	O	BITE control to down-converter GL
40	VDD			
41	**PLLLOCKG**	PIUN	I	I/P to monitor GLONASS front-end
42	**TMAG**	POL8N	O	Test PRN Pattern Magnitude o/p
43	**TSIGN**	POL8N	O	Test PRN Pattern Sign output
44	**TICO**	POL8N	O	TIC output from Master
45	**PWRRTC**	PIUN	I	RTC PWR pin sost
46	VSS			
47	**RTSA**	POL8N	O	Request To Send UART A
48	**DTRA**	POL8N	O	Data Terminal Ready UART A
49	**RIA**	PINN	I	Ring Indicator UART A
50	**CDA**	PINN	I	Carrier Detect UART A
51	**DSRA**	PINN	I	Data Set Ready UART A
52	**CTSA**	PINN	I	Clear To Send UART A
53	**DTRB**	POL8N	O	Data Terminal Ready UART B
54	**OP2A**	POL8N	O	User Defined output UART A
55	**RXA**	PINN	I	Receive Data input to Channel A of the dual UART
56	VDD			
57	**TXA**	POL8N	O	Transmit Data output from Channel A of the dual UART
58	**OP2B**	POL8N	O	User Defined output UART B
59	**RTSB**	POL8N	O	Request To Send UART B
60	**CTSB**	PINN	I	Clear To Send UART B
61	**RIB**	PINN	I	Ring Indicator UART B
62	**RXB**	PINN	I	Receive Data input to Channel B of the dual UART
63	**CDB**	PINN	I	Carrier Detect UART B
64	**DSRB**	PINN	I	Data Set Ready UART B
65	**TXB**	POL8N	O	Transmit Data output from Channel B of the dual UART
66	VSS			
67	VSS			
68	**DISCOPN**	POL8N	O	On/Off control for LNA by GPS
69	**DISCOPG**	POL8N	O	On/Off control for LNA by GLONASS
70	**TMARK**	POL16N	O	One pulse per second output
71	**MARKFB**	PIUN	I	Time Mark line driver feedback
72	VSS			

DESCRIPTION OF BUFFER TYPE

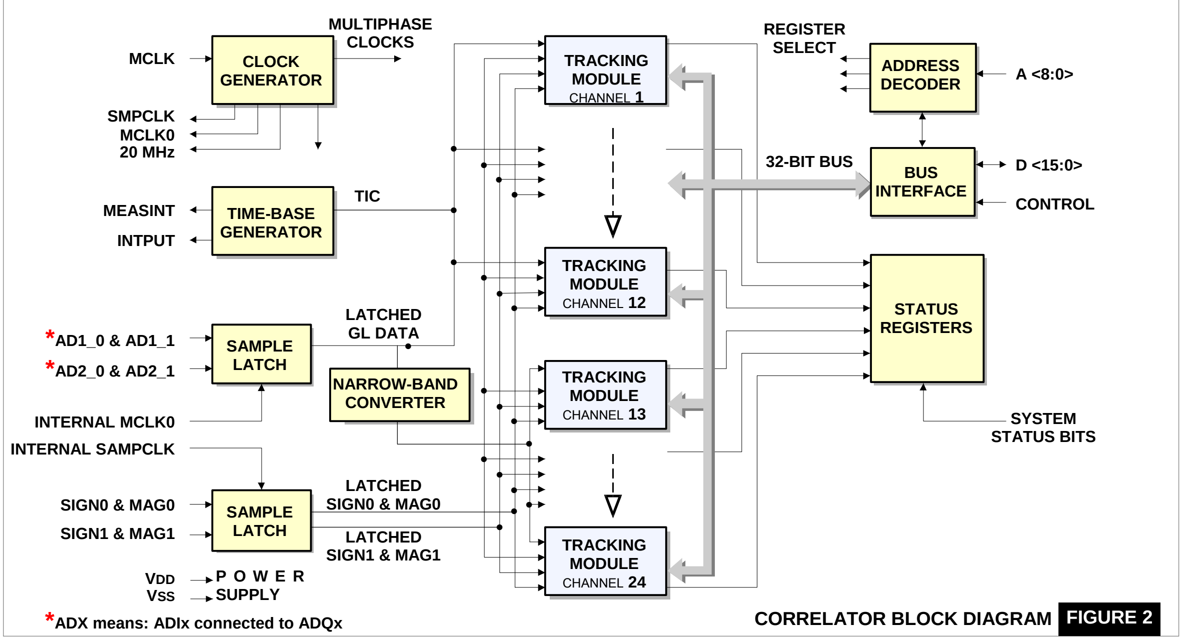
BUFFER TYPE	DESCRIPTION
PINN	Input pad
PIUN	Input pad with pull-up
PISUN	Schmitt trigger input pad with pull-up
PBL16N	CMOS 3-state output pad with input and limited slew rate (16mA)
POL8N	CMOS output pad with limited slew rate (8mA)
PO8N	CMOS output pad (8mA)

TABLE 1 CONTINUE

PIN No.	SIGNALNAME	BUFFER TYPE	DIREC-TION	DESCRIPTION
73	VDD			
74	CSBT	POL8N	O	Boot ROM chip select
75	WRRTC	POL8N	O	Write strobe external RTC
76	RDRTC	POL8N	O	Read strobe external RTC
77	RSTIN	PINN	I	Master Reset (active low)
78	INTB	PIUN	I	External interrupt B
79	IRQ	POL8N	I	Peripheral devices interrupt request
80	INTA	PIUN	I	External interrupt A
81	WRRS	POL8N	O	Write strobe external UART
82	MRES	POL8N	O	Soft reset external devices
83	BMS	PINN	I	Boot Memory Select
84	CSRTC	POL8N	O	Chip select external RTC
85	ALERTC	POL8N	O	Address latch enable external RTC
86	VSS			
87	MEAS_INT	POL8N	O	Interrupt output to microprocessor
88	RESET	POL8N	I	Master Reset (active low)
89	RESRS	POL8N	O	Hard reset external devices (High)
90	INTOUT	POL8N	O	Interrupt out to microprocessor
91	VDD			
92	CSB	POL8N	O	Chip select 2 external UART
93	CSA	POL8N	O	Chip select 1 external UART
94	RD	PINN	I	Bus control – read strobe
95	WR	PINN	I	Bus control – write strobe
96	WDI	POL8N	O	Reset external watch Dog
97	ACK	POL8N	O	Data bus ready
98	WDO	PIUN	I	External Watch Dog input
99	A9	PINN	I	Register Address, bit 9
100	A8	PINN	I	Register Address, bit 8 (Test mode, GND)
101	A7	PINN	I	Register Address, bit 7
102	A6	PINN	I	Register Address, bit 6
103	A5	PINN	I	Register Address, bit 5
104	A4	PINN	I	Register Address, bit 4
105	A3	PINN	I	Register Address, bit 3
106	A2	PINN	I	Register Address, bit 2
107	A1	PINN	I	Register Address, bit 1
108	A0	PINN	I	Register Address, bit 0
109	Vss			
110	D0	PBL16N	I/O	Data Bus, bit 0
111	D1	PBL16N	I/O	Data Bus, bit 1
112	D2	PBL16N	I/O	Data Bus, bit 2
113	D3	PBL16N	I/O	Data Bus, bit 3
114	D4	PBL16N	I/O	Data Bus, bit 4
115	D5	PBL16N	I/O	Data Bus, bit 5
116	D6	PBL16N	I/O	Data Bus, bit 6
117	D7	PBL16N	I/O	Data Bus, bit 7
118	VDD			
119	D8	PBL16N	I/O	Data Bus, bit 8
120	D9	PBL16N	I/O	Data Bus, bit 9
121	D10	PBL16N	I/O	Data Bus, bit 10
122	D11	PBL16N	I/O	Data Bus, bit 11
123	D12	PBL16N	I/O	Data Bus, bit 12
124	D13	PBL16N	I/O	Data Bus, bit 13
125	D14	PBL16N	I/O	Data Bus, bit 14
126	D15	PBL16N	I/O	Data Bus, bit 15
127	VSS			
128	VDD INT			
129	VDD INT			
130	VREF_1.8 (Output 1.8V)			
131	GND			
132	GND			
133	VSS			
134	OED7	POL12N	O	External Data Output 7
135	OED6	POL12N	O	External Data Output 6
136	OED5	POL12N	O	External Data Output 5
137	OED4	POL12N	O	External Data Output 4
138	VDD			
139	OED3	POL12N	O	External Data Output 3
140	OED2	POL12N	O	External Data Output 2
141	OED1	POL12N	O	OExternal Data Output 1
142	OED0	POL12N	O	External Data Output 0
143	VSS			
144	VDD			

FUNCTIONAL DESCRIPTION

The SR8824 is a 24-channel digital Correlator which may be used to acquire and track the GPS C/A code or the GLONASS signals. The SR8824 incorporates a 24-channel GNSS Correlator.
The SR8824 has on-chip support for the AD2106x 32-bit processors .
12 channels of the SR8824 includes independent digital GLONASS conversion to narrow-band, independent digital down-conversion to baseband, C/A and GLONASS code generation, correlation, and accumulate-and-dump registers.
Another 12 channels of the SR8824 don't includes independent digital GLONASS conversion to narrow-band.
Fig. 2 shows a block diagram of the Correlator. It consists of the following blocks:



CORRELATOR BLOCK DIAGRAM **FIGURE 2**

SOFTWARE REQUIREMENTS

The very wide variety of types of GNSS receiver needs to operate the correlator in different ways. So to accommodate this and also to allow dynamic adjustment of loop parameters, the SR8824 has been designed to use software for as many functions as possible. This flexibility means that the device cannot be used without a microprocessor closely linked to it, but as a processor is always needed to convert the output of the SR8824 into useful information this is not a significant limitation.

The software associated with the SR8824 can be divided into two separate modules:

1. Acquire and track satellite signals to give pseudo-ranges.
2. Process pseudo-ranges to give the navigation solution and format it in a form suitable for the user.

For the Navigation Solution to be possible all of the pseudoranges must have exactly the same clock error, which can then be removed iteratively to give real ranges if sufficient satellites are tracked (three if the height is known, otherwise four). This need for exact matching of timing errors explains the need for all of the complicated synchronisation between all 12 channels of the correlator.

The following relates only to the signal processing aspects of the software, to acquire and track signals from up to twelve satellites and to obtain the pseudo-ranges and the navigation message. The operation of the navigation software is not dependent on the details of the correlator, and so does not need to be included in this data sheet.

A pair of on-chip interrupt timebase signals are provided to help implement a data transfer protocol between the microprocessor and the 12-channel correlator at fixed time intervals; these signals are:

1. INTOUT - used to interrupt the microprocessor to retrieve accumulated data (1·023ms worth) - period of interrupt normally less than 1ms.
2. MEAS_INT - used to interrupt the microprocessor to retrieve Measurement data that occurs every TIC (approximately 100ms period).

These interrupts can be used to achieve instant response from the microprocessor via an Interrupt Service Routine. Otherwise software based polling scheme will be needed; the choice is set by the application. If the INTOUT interrupt is used, and perhaps also if polling is used, the data transfer rate is about twice the correlation result rate for each channel, so many transfers will not give new data. Examining the status registers before each transfer to see if new data is available and then only reading the data if it is useful can reduce bus use.

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It is important to note that the timing of each of the correlator channels will be locked to its own incoming signal and not to each other or to the microprocessor interrupts, so new data is generated asynchronously. The sampling instant of measurement data of all channels however is common to give a consistent navigation solution.

In order to acquire lock to the satellites as quickly as possible, the data from the last fix should be stored as a starting point for the next fix. It is also useful to make use of the embedded real-time clock on the chip to give a good estimate of GNSS time for the next fix; the navigation solution can be used to measure clock drift and calculate a correction for the clock to overcome ageing. The user's location (or a good estimate of it) along with the Almanac and the correct time will indicate which satellites should be searched for. These may be used to find an estimate of Doppler effects, while the previous clock error is the best available estimate of the present clock error. If this information is not available then the receiver must scan a much wider range of values, which will greatly increase the time to lock. The satellite Clock Correction and Ephemeris are needed for the navigation solution, so if a recent set is held in memory the calculations may begin as soon as lock is achieved and not need to wait for the Satellite Navigation message re-transmission (18 to 36 seconds).

❑

PACKAGE INFORMATION

PLASTIC LQFP-144 PIN